Notice of Allowability	Application No.	Applicant(s)	
	10/762,351	FUKUZAKO, SHINICHI	
	Examiner	Art Unit	
	Thuy V. Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/23/2004 & Preliminary Amendment filed 01/23/2004*.

2. ☒ The allowed claim(s) is/are *20-38*.

3. ☒ The drawings filed on *23 January 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/278,788* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 01/23/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Thuy V. Tran
Examiner
Art Unit: 2821

DETAILED ACTION

This is a response to the Applicant's filing on 01/23/2004 and preliminary amendment filed concurrently. In virtue of this filing and this preliminary amendment:

- Claims 1-19 were originally filed, and now canceled in virtue of this preliminary amendment;
- Claims 20-38 are newly added in virtue of this preliminary amendment; and thus
- Claims 20-38 are now presented in the instant application.

Allowable Subject Matter

1. Claims 20-38 are allowed.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

Prior art fails to disclose or fairly suggest:

- A drive circuit comprising (1) a first MOS transistor of a first conductive type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the input node, and (2) a second MOS transistor of the first conductivity type, the second MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate supplied with a predetermined potential level, in combination with the remaining claimed limitations as called for in independent claim 20 (claims 21-22 are allowed since they are dependent on claim 20);
- A drive circuit comprising (1) a first MOS transistor of a first conductive type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the input node, and (2) a second MOS transistor of the first conductivity

type, the second MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate supplied with a predetermined potential level, in combination with the remaining claimed limitations as called for in independent claim 23 (claims 24-25 are allowed since they are dependent on claim 20);

- A drive circuit comprising (1) a first MOS transistor of a first conductive type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the data input node, (2) a second MOS transistor of a second conductivity type, the second MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the data input node, and (3) a third MOS transistor of the first conductivity type, the third MOS transistor having a source, a drain connected to the source of the first MOS transistor, and a gate supplied with a predetermined potential level between the source potential level and the ground potential level, in combination with the remaining claimed limitations as called for in independent claim 26 (claim 27 is allowed since it is dependent on claim 26);
- A drive circuit comprising (1) a first MOS transistor of a first conductive type, the first MOS transistor having a source, a drain connected to the output node, and a gate connected to the data input node, (2) a second MOS transistor of a second conductivity type, the second MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the data input node, and (3) a third MOS transistor of the first conductivity type, the third MOS transistor having a source, a drain connected to the source of the first MOS

transistor, and a gate supplied with a predetermined potential which is less than the source potential level and more than the ground potential level, in combination with the remaining claimed limitations as called for in independent claim 28;

- A drive circuit comprising (1) a first MOS transistor of a first conductivity type, the first MOS transistor having a source, a drain connected to the output node, and a gate supplied with a predetermined potential which is less than the source potential level and more than the ground potential level, (2) a second MOS transistor of a second conductivity type, the second MOS transistor having a source connected to the source node, a drain connected to the source of the first MOS transistor, and a gate connected to the data input node, and (3) a third MOS transistor of a second conductivity type, the third MOS transistor having a source connected to the ground node, a drain connected to the output node, and a gate connected to the data input node, in combination with the remaining claimed limitations as called for in independent claim 29 (claim 30 is allowed since it is dependent on claim 29);
- A drive circuit comprising (1) an operational amplifier having an inversion terminal to which a reference voltage is applied, a non-inversion terminal and an output terminal, (2) a first MOS transistor of a first conductivity type, wherein the first MOS transistor has a source, a drain connected to the non-inversion terminal of the operational amplifier and a gate connected to the output terminal of the operational amplifier, and (3) a second MOS transistor of the first conductivity type, wherein the second MOS transistor has a source connected to a source node supplied with a source potential, a drain connected to the source of the first MOS transistor, and a

gate connected to a gate node supplied with a gate potential level, in combination with the remaining claimed limitations as called for in independent claim 31 (claims 32-34 are allowed since they are dependent on claim 31); and

- A drive circuit comprising (1) an operational amplifier having a non-inversion terminal to which a reference voltage is applied, an inversion terminal and an output terminal, (2) a first MOS transistor of a first conductivity type, wherein the first MOS transistor has a source, a drain connected to the inversion terminal of the operational amplifier and a gate connected to the output terminal of the operational amplifier, and (3) a second MOS transistor of the first conductivity type, wherein the second MOS transistor has a source connected to a ground node supplied with a ground potential level, a drain connected to the source of the first MOS transistor, and a gate connected to a source node supplied with a source potential level, in combination with the remaining claimed limitations as called for in independent claim 35 (claims 36-38 are allowed since they are dependent on claim 35).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Citation of relevant prior art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Tam (Pub. No.: US 2002/0047817 A1) discloses a display device and electronic driving apparatus.

Prior art Kasai (U.S. Patent No. 6,750,833) discloses a system and methods for providing a driving circuit for active matrix displays.

Prior art Shiina et al. (U.S. Patent No. 6,040,827) discloses a driver circuit.

Prior art Orita et al. (U.S. Patent No. 6,028,573) discloses a driving method and apparatus for display device.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thuy V. Tran
Examiner
Art Unit 2821

09/28/2004